REMARKS

Applicants respectfully request consideration of the subject application. This Response is submitted in response to the Office Action mailed May 2, 2006. Claims 1-30 stand rejected. In this Amendment, claims 1, 20, 23 and 28 have been amended and claims 4, 22 and 30 have been cancelled. No new matter has been added.

35 U.S.C. §§ 102 and 103 Rejections

The Examiner has rejected claims 1 and 20 under 35 U.S.C. § 102(b) as being anticipated by Oida, et al. (U.S. Patent No. 5,647,917, hereinafter "Oida"). The Examiner has rejected claims 2-4, 6, and 7 under 35 U.S.C. § 103(a) as being unpatentable over Oida. The Examiner has rejected claims 8-10 and 22-23 under 35 U.S.C. § 103(a) as being unpatentable over Sato (U.S. Patent No. 6,375,738, hereinafter "Sato") in view of Oida. The Examiner has rejected claims 11-16 and 24-30 under 35 U.S.C. § 103(a) as being unpatentable over Sato in view of Oida. The Examiner has rejected claims 5 and 17-19 and 24-30 under 35 U.S.C. § 103(a) as being unpatentable over Sato in view of Oida and Henley, et al. (U.S. Patent No. 6,558,802, hereinafter "Henley").

Claims 1-3, 5-9 and 17-19

The cited art fails to teach or suggest, inter alia, as claimed in claim 1: "notching the wafer to form an orientation indication feature at an angle greater

than 0 degrees from a crystal plane that is perpendicular to a horizontal surface of the wafer." Similar limitations are included in independent claims 7 and 17.

Oida is directed to a method of cutting wafers at an off-angle to suppress the occurrence of hillocks. In particular, Oida discloses a specific method for calculating an optimum off-angle for preventing the hillocks.

Sato is directed to a method of making a semiconductor article in which differing semiconductor layers are grown on a single crystal substrate, and subsequently bonding a support substrate to the single crystal substrate. The grown semiconductor layers differ in kind and/or concentration of an impurity.

Henley is directed to a method of forming a hybrid wafer in which a high-quality bond is formed between a thin film and a target wafer during a high-temperature annealing process.

Neither Oida, Sato, nor Henley disclose notching or marking a wafer, as presently claimed. The Examiner has pointed to no teaching in the art for the above limitations. Instead, the Examiner submits that "in the absence of unexpected results, it would have been obvious to one of ordinary skill in the art to determine through routine experimentation the optimum, operable orientations to be cut in the Oida et al reference in order to create the desired wafer orientation as the reference does teach that different orientation can be use[d] and are within the skill of the art." Applicants respectfully disagree.

As explained in the specification, the purpose of the orientation indication feature is to ensure that the devices are oriented in the same direction along the

crystal planes in each batch of the wafers and consistently within a single wafer. Also, as explained in the specification, one of the parameters that results in the varied crystal orientations is the orientation indication feature that is used to align the wafer during processing, which ultimately results in certain properties of the substrates being changed. In particular, the properties that may change include, for example, the etching rate and characteristics, the oxidation rate and characteristics, the hardness of the wafer in a particular direction, and the mobility of electrons within the wafer in a particular direction.

Accordingly, Applicants respectfully request the Examiner point to a reference for the claimed limitations.

Thus, the cited art fails to disclose all of the limitations of independent claims 1, 7 and 17.

Claims 10-16 and 23-27

The cited art fails to teach or suggest, inter alia, as claimed in claim 10: "providing a second semiconductor wafer having a second crystal orientation that is different from the first crystal orientation." Similar limitations are included in independent claim 23.

Neither Oida, Sato, nor Henley disclose bonding wafers having differing crystal orientations, as presently claimed. The Examiner has pointed to no teaching in the art for the above limitations. Instead, the Examiner submits that "It would have been obvious to one of ordinary skill in the art to modify the Sato

reference by the teachings of Oida et al reference to use different orientation in order to place a epitaxially structure of one orientation on a substrate with a different one changing the device properties." Applicants respectfully disagree.

As explained in the specification, in addition to properties being varied by affecting the crystal orientation, properties can be varied by varying crystal orientations of wafers that are bonded together. In one particular embodiment, the variability may be valuable in instances where a thin device layer is used combination with a mechanically strong silicon carbide handle wafer or where transistors are formed on the device layer and MEM's are formed on the handle wafer.

Accordingly, Applicants respectfully request the Examiner point to a reference for the claimed limitations.

Thus, the cited art fails to disclose all of the limitations of independent claims 10 and 23.

Claims 20-21 and 28-29

The cited art fails to teach or suggest, inter alia, as claimed in claim 20: "increasing electron mobility within a transistor channel on a semiconductor wafer by forming the semiconductor wafer to have a non-standard crystal orientation." The cited art fails to teach or suggest, inter alia, as claimed in claim 28: "a silicon substrate having a face centered cubic crystal lattice and a

horizontal crystal plane of the lattice that is not a [100], [110], or [111] crystal plane."

Neither Oida, Sato, nor Henley disclose increasing electron mobility within a transistor channel by forming a wafer having a non-standard crystal orientation or a silicon substrate that has a face centered cubic crystal lattice and a horizontal crystal plane that is not a [100], [110], or [111] crystal plane.

As explained in the specification, one of the parameters that results in the varied crystal orientations is forming a wafer having a non-standard crystal orientation (e.g., a face centered cubic crystal lattice and a horizontal crystal plane that is not a [100], [110], or [111] crystal plane), which ultimately results in certain properties of the substrates being changed. In particular, the properties that may change include, for example, the etching rate and characteristics, the oxidation rate and characteristics, the hardness of the wafer in a particular direction, and the mobility of electrons within the wafer in a particular direction.

Thus, the cited art fails to disclose all of the limitations of independent claims 20 and 28.

Therefore, neither Oida, Sato, Henley nor combinations thereof disclose or suggest the claimed limitations of independent claim 1, 7, 10, 17, 20, 23 and 28. Claims 2-3, 5-6, 8-9, 11-16, 18-19, 21, 24-27 and 29 depend, directly or indirectly, from one of the foregoing independent claims.

Applicant, accordingly, respectfully requests withdrawal of the rejections of claims 1-30 under 35 U.S.C. §§ 102 and 103.

Applicant respectfully submits that the present application is in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call Jennifer Hayes at (408) 720-8300.

Please charge any shortages and credit any overages to Deposit Account No. 02-2666. Any necessary extension of time for response not already requested is hereby requested. Please charge any corresponding fee to Deposit Account No. 02-2666.

Respectfully submitted,

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